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Documentation on design automation subjects – The Bird's-eye View of Design Languages (BVDL)

Documentation sur les sujets concernant l'automatisation de la conception – Langages BVDL (Bird's-eye View of Design Languages)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – THE BIRD'S-EYE VIEW OF DESIGN LANGUAGES (BVDL)

FOREWORD

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IEC 62856, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology:

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
91/1085/DTR	91/1101/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

The automation of design and manufacturing technologies in electronic industries has been evolving world-wide for over three decades with remarkable development speed. Electronic design automation (EDA) technology enables the conceptualization, implementation and validation of electronic systems, that is, transforms the ideas and objectives of the system designers into manufacturable and testable representations in a cost-effective way. It is classified into three key categories such as design methodologies, design libraries and design tools. Standardization involves computer-sensible representations throughout the overall design processes which integrate design libraries and design tools to build a design ecosystem.

In the semiconductor industry EDA technologies have been substantially contributing to the unprecedented industry growth for three decades. To emerging new product lines such as microcontroller, microprocessor, ASIC, FPGA, memories, analog and mixed-signal and System on a chip (SoC) they have been continuously providing a wide range of solutions to meet critical requirements on design productivity enhancement and design quality improvement.

The EDA technical committee (EDA-TC) was formed in JEITA in 1990 in order to take initiatives for international EDA standardization in Japan. Since then, it has been contributing design language standardization such as EDIF, VHDL, Verilog HDL, Delay and Power Calculation (DPC), System C, System Verilog and Power Format, which led to forming the new working group at which experts from the industry and academia were invited and to work with IEC TC93, IEEE DASC, Accellera, Open SystemC Initiatives (OSCI) and others. After having been active for over two decades the need was felt for a bird’s-eye view of the existing tens of design languages, and to enhance or develop them in order to set the strategy towards international EDA standardization. EDA-TC initiated the project in early 2009 to develop the Bird’s-eye View of Design Languages (BVDL) spreadsheet documentation. It developed the first version in March 2010, in order to have an important participation of design technology experts from the semiconductor industry and academia. It finalized the BVDL documentation combined with the spreadsheet as a JEITA technical report in March 2011.

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – THE BIRD'S-EYE VIEW OF DESIGN LANGUAGES (BVDL)

1 Scope

The BVDL originally aims to make full use of planning and decision-making on EDA standardization activities for a technical expert as well as a manager in JEITA. It facilitates the understanding of the various design languages to show their positioning and features. Also it provides easy overviews of each design language for a newcomer to the EDA standards community and/or for a designer as a user of an EDA design ecosystem. Especially for a design language developer that aims to directly join design language development and voting for standardization, it provides metrics to check for duplication among similar languages, consistency to develop the design ecosystem and future challenges for design languages.

EDA standards provide a mechanism to define common semantics for electronic design ecosystems among various design tools depicted in Figure 1. The state-of-the-art standards are classified into hardware description languages, hardware verification languages, electronic system level design languages, library formats, design constrain formats, interface formats with manufacturing and testing, design data exchange formats, data models and application procedure interfaces (API), etc. Therefore they are generally called standard design languages in a narrow sense. The semiconductor industry has been facing new design complexity barriers and is today facing unprecedented complexities brought by the convergence of product features in terms of silicon process technology, system technology, high gate count and embedded software incorporation. This new design complexity requires integrated EDA solutions and at the same time impacts design ecosystem and standard design languages as well. So a new design language development or new features enhancement to an existing design language is needed. As a result tens of design languages, which might be classified into de jure standard language, de facto standard language, forum standard language and common language used in some community, are developed, enhanced or actually used in the industries, academia and communities world-wide.

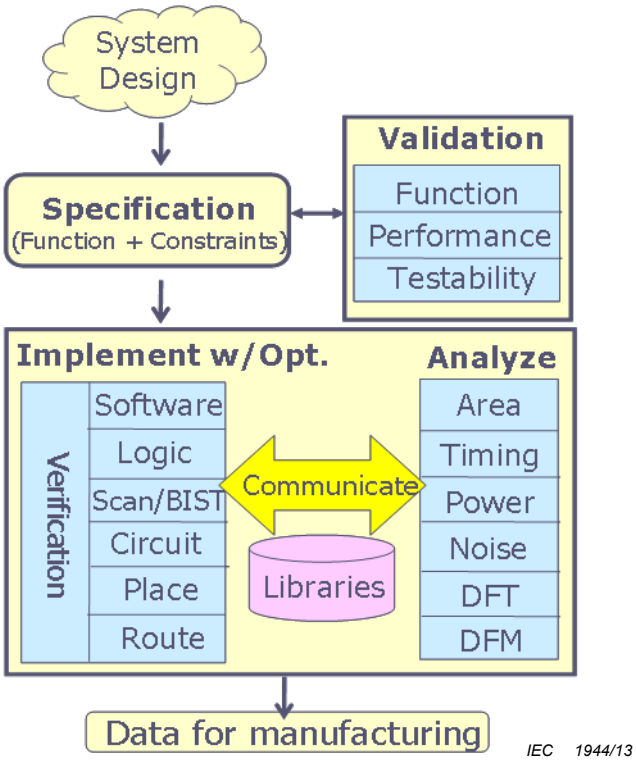

Figure 1 – Electronic design ecosystem

This technical report describes features for existing design languages, as well as for enhancing and newly developing design languages belonging to the defined design processes of System on a chip (SoC) which ranges from system level design, SoC design implementation and verification, IP block creation and analog block design down to interface data preparation for manufacturing. These simplified design processes might not become obsolete despite the remarkable speed of the evolution of electronic design automation and seem easier to understand for a non-EDA expert.

Thirty-three design languages have been chosen and each feature of their latest version as of March 2011 is reflected in this report:

UML

Esterel

Rosetta

SystemC

SystemC-AMS

IBIS

CITI

TouchStone

BSDL

System Verilog

VHDL

Verilog HDL

UPF

CPF

e language
PSL
FSDB
SDC
DEF
Open Access
SDF
GDS II
OASIS
STIL
WGL
Verilog-A
Verilog-AMS
SPICE
VHDL-AMS
LEF
Liberty
CDL
IP-XACT.